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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/701,261	11/03/2003	Jui-Feng Ko	JCLA7806	6081

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EXAMINER	
SHERMAN, STEPHEN G	
ART UNIT	**PAPER NUMBER**
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/701,261	KO ET AL.	
	Examiner	Art Unit	
	Stephen G. Sherman	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed the 3 April 2007. Claims 1 and 3-7 are pending.

Response to Arguments

2. Applicant's arguments filed 3 April 2007 have been fully considered but they are not persuasive.

On page 5 of the applicant's response the applicant argues the rejection of claims 1 and 3-7 under 35 USC 102 as being anticipated by Jennings. The applicant states in the 4th paragraph under the heading "*Claim Rejections 35 U.S.C. 102*" that Jennings fails to teach the claimed limitation of "wherein the control chip is able to spread out the frequency of an electromagnetic interference signal according to an algorithm". The applicant's argument to support this state is that Jennings spreads out the input clock signal rather than "frequency of an electromagnetic interference signal" as required by the claimed invention. The applicant then admits that Jennings also concerns to reduce EMI, however, that Jennings concern is to operate on the entire input signal rather than the "frequency of an electromagnetic interference signal". The examiner respectfully disagrees.

The examiner asserts that there is nothing in the claim language that precludes the examiner from stating that the clock signal is the "electromagnetic interference

signal". As admitted by the applicant, Jennings discloses of modulating a clock signal in order to reduce EMI, and therefore by spreading out the frequency of the clock signal Jennings is spreading out the frequency of EMI. Therefore, it can be concluded that the clock signal contains the electromagnetic interference signal and since the clock signal is spread out then the electromagnetic interference signal is spread out. Thus, since the claim does not define the electromagnetic interference signal the examiner's use of the clock signal as the claimed "electromagnetic interference signal" is justified. Furthermore, the applicant's specification does not define what an "electromagnetic interference signal" is, and therefore the clock signal of Jennings can be considered an "electromagnetic interference signal".

Also, the applicant's invention, as shown in Figure 3, takes a CLK in and then produces a modulated clock signal. The applicant also states in paragraph [0022] that a conventional SSCG spreads out an electromagnetic interference signal and that the only thing that is new in their invention is that the center frequency is able to be changed by an algorithm. Thus since Jennings discloses a SSCG which can change the modulation frequency, then according to the applicant's specification Jennings would be spreading out an electromagnetic interference signal, which further proves that Jennings anticipates the claimed invention [See also column 1, lines 51-65 of Jennings which explains that SSCG are for spreading the spectrum of radiated emission of a clock signal, i.e. an electromagnetic interference signal.].

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1 and 3-7 are rejected under 35 U.S.C. 102(e) as being anticipated by Jennings (US 6,697,416).

Regarding claim 1, Jennings discloses a control chip built inside an integrated circuit for reducing electromagnetic interference (Figure 3 is s block diagram of a SSCG as explained in column5, lines 46-49.), wherein

the control chip is able to spread out the frequency of an electromagnetic interference signal according to an algorithm (Figure 3 shows that the MODULATOR (M) 20 receives a FREQUENCY MODULATION CONTROL word which programs a frequency, which contributes to the output from the MODULATOR 20 to produce an unfiltered spread spectrum clock and eventually the output SPREAD SPECTRUM CLOCK , as explained in column 5, lines 53-60, column 6, lines 29-37, and column 7, lines 1-9.),

wherein the control chip picks up the algorithm from an external bus (Figure 3 shows that MODULATOR (M) 20 receives the FREQUENCY MODULATION CONTROL externally, as is further shown in Figure 4 through the inputs S0-S4 which are input from an external source.), and

the electromagnetic interference signal at each frequency are modulated according to a corresponding spread out width (Figure 6 and column 9, lines 26-34 explain that at every frequency in deviation from the center frequency the signal is modulated according to the width set as shown in the figure.).

Regarding claim 3, Jennings discloses a control chip for reducing electromagnetic interference (Figure 3 is s block diagram of a SSCG as explained in column5, lines 46-49.), comprising:

a software phase lock loop built inside the control chip for receiving a clock signal and spreading out the frequency of an electromagnetic interference signal according to an algorithm received from an external bus (Figure 3, which is an SSCG which allows for changes for the output center frequency via software as explained in column 4, lines 50-60, shows that the MODULATOR (M) 20 receives a FREQUENCY MODULATION CONTROL word which programs a frequency, which contributes to the output from the MODULATOR 20 to produce an unfiltered spread spectrum clock and eventually the output SPREAD SPECTRUM CLOCK from the PLL, as explained in column 5, lines 53-60, column 6, lines 29-37, and column 7, lines 1-9. Figure 3 shows that MODULATOR (M) 20 receives the FREQUENCY MODULATION CONTROL externally, as is further

shown in Figure 4 through the inputs S0-S4 which are input from an external source.), wherein the electromagnetic interference signal at each frequency are modulated according to a corresponding spread out width (Figure 6 and column 9, lines 26-34 explain that at every frequency in deviation from the center frequency the signal is modulated according the width set as shown in the figure.); and

a bus coupled to the software phase lock loop for inputting the algorithm (Figure 4 shows the input terminals S0-S4 which are used to input the external FREQUENCY MODULATION CONTROL word, where this external signal would be input from a signal line, i.e. a bus.).

Regarding claim 4, Jennings discloses the control chip of claim 3, wherein the frequency of the electromagnetic interference signal and the spread out width at that frequency is set by the algorithm within the software phase lock loop (Column 5, lines 53-60, column 6, lines 29-37, and column 7, lines 1-9 explain that the FREQUENCY MODULATION CONTROL word is used to produce the output from the modulator 20, which is in turn used to produce the output SPREAD SPECTRUM CLOCK, which means that it sets the frequency and spread out width obtained in Figure 6.).

Regarding claim 5, Jennings discloses an application specific integrated circuit for reducing electromagnetic interference (Figure 3 is s block diagram of a SSCG as explained in column5, lines 46-49.), comprising:

a first input terminal for receiving a clock signal (Figures 3 and 4 show the reference source input which is explained in column 5, lines 49-53 to be an input clock.); and

a second input terminal for receiving an algorithm from an external bus (Figure 4 shows the input terminals S0-S4 which are used to input the external FREQUENCY MODULATION CONTROL word, where this external signal would be input from a signal line, i.e. a bus.); and

a software phase lock loop coupled to the first input terminal and the second input terminal for spreading out the frequency of an electromagnetic interference signal according to the clock signal and an algorithm (Figure 3, which is an SSCG which allows for changes for the output center frequency via software as explained in column 4, lines 50-60, shows that the MODULATOR (M) 20 receives a FREQUENCY MODULATION CONTROL word which programs a frequency, which contributes to the output from the MODULATOR 20 to produce an unfiltered spread spectrum clock and eventually the output SPREAD SPECTRUM CLOCK from the PLL, as explained in column 5, lines 53-60, column 6, lines 29-37, and column 7, lines 1-9, where the PLL is coupled to the reference source input and the FREQUENCY MODULATION CONTROL word through the accumulator 21 and the modulator 20.),

wherein the electromagnetic interference signal at each frequency are modulated according to a corresponding spread out width (Figure 6 and column 9, lines 26-34 explain that at every frequency in deviation from the center frequency the signal is modulated according the width set as shown in the figure.).

Regarding claim 6, this claim is rejected under the same rationale as claim 4.

Regarding claim 7, Jennings discloses a method of reducing the strength of an electromagnetic interference signal (Figure 3 is s block diagram of a SSCG as explained in column5, lines 46-49.), comprising the steps of:

receiving an algorithm from an external bus Figure 3 shows that MODULATOR (M) 20 receives the FREQUENCY MODULATION CONTROL externally, as is further shown in Figure 4 through the inputs S0-S4 which are input from an external source.);

determining a specified frequency of the electromagnetic interference signal and a corresponding spread out width at that frequency according to the algorithm (Column 5, lines 53-60, column 6, lines 29-37, and column 7, lines 1-9 explain that the FREQUENCY MODULATION CONTROL word is used to produce the output from the modulator 20, which is in turn used to produce the output SPREAD SPECTRUM CLOCK, which means that it sets the frequency and spread out width obtained in Figure 6.); and

spreading out the electromagnetic interference signal according to the spread out width using the specified frequency as the center of spreading (Figure 6 and column 9, lines 26-34 explain that at every frequency in deviation from the center frequency the signal is modulated according the width set as shown in the figure.).

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SS

19 April 2007

AMR A. AWAD
SUPERVISORY PATENT EXAMINER